ISSCC 2016 Reports Program (2016/2/17)

Session Chair	Time		Title	Speaker(Affiliation)
	9:30 9:35		Opening	Takeshi Yamamura (Fujitsu Laboratories)
	9:35 10:00		Review of ISSCC 2016	Atsuki Inoue (Fujitsu Laboratories)
Professor Iizuka (Univ. of Tokyo)	10:00 10:25	4.4	A 197mW 70ms-Latency Full-HD 12-Channel Video-Processing SoC for Car Information Systems	Seiji Mochizuki (Renesas System Design)
	10:25 10:50	4.5	A 16nm FinFET Heterogeneous Nona-Core SoC Complying with ISO26262 ASIL-B: Achieving 10^-7 Random Hardware Failures per Hour Reliability	Chikafumi Takahashi (Renesas System Design)
	10:50 11:15	7.2	4Mb STT-MRAM-Based Cache with Memory-Access-Aware Power Optimization and Write-Verify-Write / Read-Modify-Write Scheme	Hiroki Noguchi (Toshiba)
	11:15 12:05		(Invited) 5G Technologies and Development in 2020 and Beyond	Takehiro Nakamura (NTT Docomo)
	12:05 13:30		Lunch	
Professor Ikeda (Univ. of Tokyo)	13:30 13:45	6.6	A 1280×720 Single-Photon-Detecting Image Sensor with 100dB Dynamic Range Using a Sensitivity-Boosting Technique	Mitsuyoshi Mori Manabu Usuda (Panasonic)
	13:45 14:00	6.7	A 1.2e- Temporal Noise 3D-Stacked CMOS Image Sensor with Comparator-Based Multiple-Sampling PGA	Kei Shiraishi (Toshiba)
	14:00 14:25	28.3	CMOS Biosensor IC Focusing on Dielectric Relaxations of Biological Water with 120GHz and 60GHz Oscillator Arrays	Takeshi Mitsunaka (Sharp)
	14:25 14:50	7.7	A 768Gb 3b/cell 3D-Floating-Gate NAND Flash Memory	Tomoharu Tanaka (Micron)
	14:50 15:15	19.7	A 65nm CMOS ADPLL with 360µW 1.6ps-INL SS-ADC-Based Period- Detection-Free TDC	Akihide Sai Satoshi Kondo (Toshiba)
	15:15 15:40	3.5	A 56Gb/s NRZ-Electrical 247mW/lane Serial-Link Transceiver in 28nm CMOS	Takayuki Shibasaki (Fujitsu Laboratories)
	15:40 16:15		Break	
Professor Ito (Tokyo Institute of Tech.)	16:15 16:40	13.3	A 56Gb/s W-Band CMOS Wireless Transceiver	Korkut Tokgoz Kenichi Okada (Tokyo Institute of Tech.)
	16:40 16:55	13.6	A 42Gb/s 60GHz CMOS Transceiver for IEEE 802.11ay	Rui Wu Kenichi Okada (Tokyo Institute of Tech.)
	16:55 17:20	20.1	A 300GHz 40nm CMOS Transmitter with 32-QAM 17.5Gb/s/ch Capability over 6 Channels	Kosuke Katayama (Hiroshima Univ.)
	17:20 17:45	26.1	A 5.5mW ADPLL-Based Receiver with Hybrid-Loop Interference Rejection for BLE Application in 65nm CMOS	Hidenori Okuni (Toshiba)
	17:45 18:00	26.5	A 0.7V 1.5-to-2.3mW GNSS Receiver with 2.5-to-3.8dB NF in 28nm FD-SOI	KenYamamoto Yuya Kondo (Sony)
	18:00 18:10		Closing	Hideto Hidaka (Renesas Electronics)

Tokyo Institute of Technology Ookayama Campus West Building 9 2nd Floor

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